Abstract of the Disclosure:

Each memory cell is a memory transistor which is provided on a top side of a semiconductor body and has a gate electrode which is arranged in a trench located between a source region and a drain region that are formed in the semiconductor material. The gate electrode is separated from the semiconductor material by a dielectric material. At least between the source region and the gate electrode and between the drain region and the gate electrode, there is an oxide-nitride-oxide layer sequence. The layer sequence is provided for the purpose of trapping charge carriers at the source and the drain.

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